

REMARKS

Claims 8, 9 and 11-13 are pending in this application. By this Amendment, claim 8 has been amended to incorporate the features of claim 10, and claim 10 has been correspondingly canceled. Support for the amendment to claim 8 can be found, for example, in previously presented claim 10 as well as at pg. 8, lines 20-28 of the specification and in Figs. 10-12. Thus, no new matter has been added.

I. Allowable Subject Matter

Applicants appreciate the allowance of claim 13. Applicants respectfully submit that claims 8, 9, 11 and 12 are also allowable for at least the reasons presented below.

II. 35 U.S.C. §103 Rejection

The Office Action rejects claims 8-12 under 35 U.S.C. §103(as) as being obvious over U.S. Patent Application Publication No. 2002/0047172 (hereinafter "Reid") in view U.S. Patent No. 5,835,256 (hereinafter "Huibers"), and further in view of WO 00/33089 (hereinafter "Mathieu"). This rejection is respectfully traversed.

Claim 8 has been amended to incorporate the features of claim 10. Specifically, claim 8 has been amended to recite "wherein the planarization step successively comprises a chemical mechanical polishing sub-step of the embedding layer **and an etching sub-step of the embedding layer** so that the front faces of the sacrificial layer and of the embedding layer form a common flat surface" (emphasis added). Reid, Huibers, and Mathieu, taken alone or in combination, fail to disclose or render obvious at least the above-quoted feature of claim 8.

The Office Action alleges, at pg. 5, that Reid discloses the features of claim 10 (which have been incorporated into claim 8). However, the Office Action fails to cite to any portion of Reid in support of this allegation.

Reid, taken alone or in combination with Huibers and Mathieu, fails to disclose or render obvious a planarization step that includes a chemical mechanical polishing sub-step

and an etching sub-step. As shown in Fig. 2B, Reid discloses depositing a sacrificial layer 42 of amorphous silicon by a PECVD or PVD process on a circuit substrate 40. Reid discloses that the sacrificial layer 42 may then be patterned to form an aperture. A plug layer 43, which is a metal compound, is then deposited over the sacrificial layer 42 so as to fill the aperture. (See paragraph [0023]). Deposition of the plug layer 43 is then followed by a chemical mechanical polishing step to form a plug 44 so that the plug 44 and the sacrificial layer 42 having a smooth surface 45. (See paragraph [0023]).

Reid only discloses that a single step of chemical mechanical polishing is used to polish layers 43 and 42 to form a smooth surface. Reid fails to disclose or render obvious a planarization step that successively comprises a chemical mechanical polishing sub-step of the embedding layer **and an etching sub-step of the embedding layer** so that the front faces of the sacrificial layer and of the embedding layer form a common flat surface, as recited by claim 8. In contrast, according to an embodiment of the present disclosure as recited by claim 8, the planarization step includes chemical mechanical polishing of the embedding layer 6 (Fig. 13) followed by etching of the embedding layer 6 to form a common smooth surface with the sacrificial layer 2 (Fig. 14).

Moreover, a planarization step that includes a chemical mechanical polishing step followed by an etching step would be inconsistent with the teachings of Reid as it cannot be used to produce a common smooth surface. Reid discloses that the sacrificial layer 42 is amorphous silicon and the plug layer 43 is a metal compound. Thus, the sacrificial layer 42 and the plug layer 43 are different materials and both layers are not smooth. Thus, a planarization step that includes an etching sub-step would require etching of the plug layer 43 and the sacrificial layer 42. The sacrificial layer 42 and the plug layer 43 would have different etching rates because they are formed from different materials, and a common smooth surface would not be attainable.

Although, Reid discloses that the sacrificial layer 42 may be any suitable sacrificial material, it is understood in the art that the plug layer 43 and the sacrificial layer 42 must be formed of different materials in order for the sacrificial layer 42 to be removed through dissolution and the plug layer 43 to remain (see paragraph [0024]).

Further, Reid, taken alone or in combination with Huibers and Mathieu, fails to disclose or render obvious "deposition, on at least part of the substrate and on at least part of the front face of the sacrificial layer, of the embedding layer presenting a larger thickness than the thickness of the sacrificial layer, **the embedding layer surrounding the sacrificial layer**," (emphasis added) as recited by claim 8. As clearly shown in at least Fig. 2B of Reid, the plug layer 43 (alleged embedding layer) is not deposited so as to surround the sacrificial layer 42.

Further, Huibers and Mathieu fail to at least cure the deficiencies of Reid discussed above.

Therefore, claim 8 is patentable over the applied combination of references. Claims 9, 11 and 12 are also patentable for at least their dependency from claim 8 as well as for the additional features they recite.

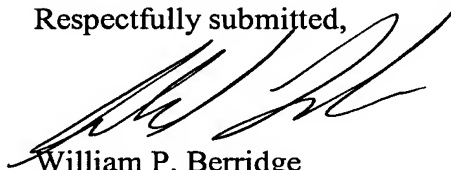
Accordingly, withdrawal of the rejection is respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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